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EMC Testing

DC-DC converter – SYNC pin from EMC perspective

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Abstract

Among the engineering challenges and trade-offs, beside the technical ones, there is always the system cost. The main design goal is typically to achieve what the marketing department asks for, with the minimal cost. This will enable a cheaper product and would allow a better revenue margin by selling the product in the market. The SYNC pin is a typical feature offered by high current DC-DC converters (typically from 2A and higher) that enables reducing the size of the input capacitance in case multiple DC-DC converters are required. The article will introduce how and why the SYNC feature is used, and which benefit may bring also from the EMC perspective.

SYNC feature by DC-DC converters

Figure 1 depicts a simple use case that could represent a typical point of load requirement for a small FPGA, made of two buck converters IC1 and IC2. In particular it is not unusual that the required FPGA voltages will be in the range of 1V. This causes an increase of I_{OUT} (compared to I_{IN}), which in certain applications may also get up to 20-30A for the V_{CORE} voltage that goes down to 0.7-0.9V. The application in Figure 1 shows that each DC-DC converter has an input capacitor (C_1 and C_2) but you also has C_B, that may represent the output capacitor of the previous DC-DC converter that decreases the voltage from 12V-24V down to 3.3V-5V or simply a bulk capacitor that stores enough energy for the DC-DC converters in addition to C_1 and C_2.

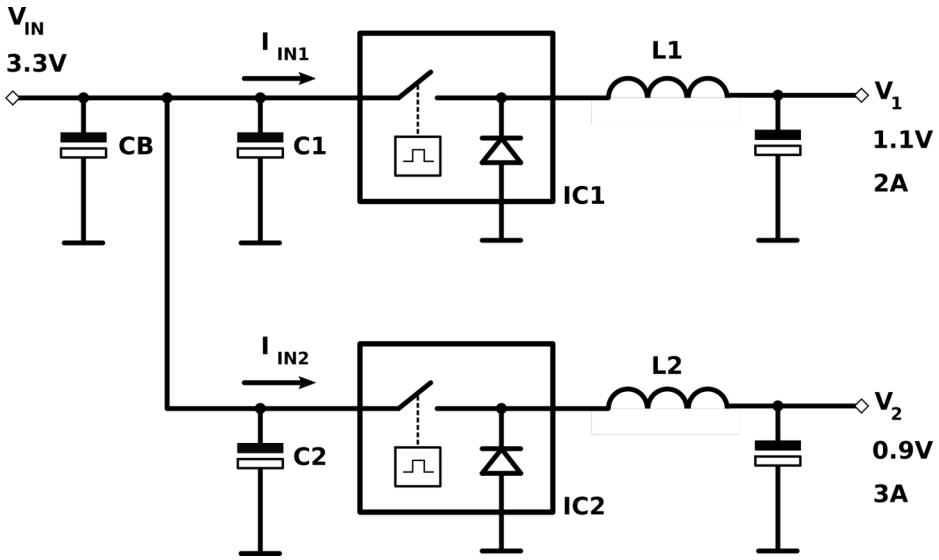

Figure 1: *Typical use case with 2 DC-DC converters.*

The DC-DC converters for the point of load, may work at a switching frequency that is internally generated by the converter itself. This simplifies the schematic but it means that IC1 and IC2 internal switches may actually be switched at the same time. If this would be the case the current I_{IN1} and I_{IN2} will be summed up. Considering that the DC-DC converter solution may be spread on a certain area, it may mean that most of the energy will be delivered first by C_1, C_2, C_B, before the main source of energy may react. This is also the reason why C_1, C_2, C_B, are typically placed close to the DC-DC converters. The

right value of those capacitors depends on the total current that must be provided in the worst case scenario and the allowed ripple. In Figure 1 the worst case would be related to the current peak of each DC-DC converter output. Indeed, as mentioned, both IC1 and IC2 switches may be closed, in the worst case, at the same time. Considering an efficiency for the converters of 90% and an input voltage of 3.3V, this will be reflected in the input having I_{IN1}=0,73A and I_{IN2}=0.9A, thus a total current of 1.63A. Depending on the DC-DC converters that are used, you need always to guarantee that the input voltage will remain within a certain range to avoid an excessive output ripple and voltage droop that may even cause an under voltage failure on the input side. Considering the capacitors total capacitance, together with the current scenario required by the application, you can determine a first optimal value for the required C. In the lab, you can trim the right value by doing the load and line transient tests on the DC-DC converter solution.

The worst scenario we have depicted, can be actually relaxed if the DC-DC converter would have SYNC pins. Indeed you can synchronize the switching frequency of both, making sure that the current peaks will not appear at the same time. This does not mean that the worst case would be only function of the higher current among the two DC-DC converters but it would be lower than the sum of it. Indeed, you need to keep into account that if you have a current peak on the first DC-DC converter and right after a peak on the second one, the bulk capacitor C_B is not fully charged. This scenario can easily happen if a simple 180° clock shift, using a simple NOT logic for one SYNC pin, is used as shown in Figure 2.

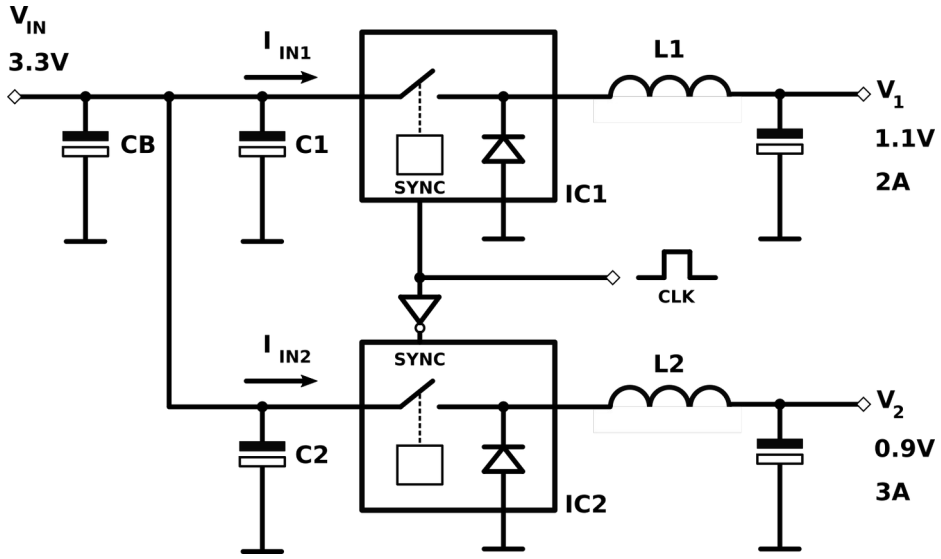

Figure 2: *Typical SYNC clock for 2 DC-DC converters.*

The use of the SYNC clock (CLK), enables reducing the input current peak that C_1, C_2, C_B, will see, thus it will allow a smaller amount of capacitance to keep the input voltage relatively constant.

From EMI perspective this is a great advantage since the conductive noise gets reduced as well. In particular the differential conductive noise, that depends mostly on the input capacitor and I, is reduced. The conductive noise gets reduced for two reasons:

- The conductive noise is relatively proportional to the input current, so the higher is the input current the higher will be the conductive noise.
- The differential noise is linked to the capacitors ESR (Equivalent Series Resistance) and the current that flows into it. Thus reducing the current that "flows" via the capacitor, reduces the differential noise.

To better understand the influence of the ESR, we have to recap what the capacitor is and where the ESR is connected to. Figure 3 shows the details of an ideal capacitor and a real one with the ESR in series (other stray elements are neglected).

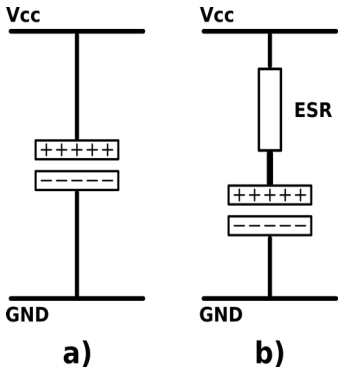

Figure 3: *Ideal capacitor a) real capacitor with ESR b).*

First of all, it is important to highlight that within a capacitor there is an insulator, thus when we say that a current flows within it, it is just an easy representation of what is happening. No current really flows through the capacitor, but rather charges go in and out from the plates upon a voltage change on the input.
If the capacitor is an ideal one, if we have an input voltage ripple due to the DC-DC converter switching, the capacitor can provide the required energy very fast, without problems. If the voltage source for the DC-DC converter is ideal, we will not even see the input voltage ripple. A real capacitor will not be that fast, since there is an ESR in serie that creates a certain friction to the moving charges. Furthermore the ESR, any time there is a current going in and out from the capacitor, will have a voltage droop. This voltage would be seen as differential voltage going up and down due to the input voltage variation. This will be seen as differential conductive noise generated by the system. Due to the differential equation that describes the charging and discharging process of the capacitor, the differential noise increases with the ESR but with an exponential function, as the charging voltage process of the capacitor.

Out of it, to reduce the conductive noise, if there is the option to sync the DC-DC converters, it is a good idea to use that feature to reduce the input current. This current reduction will help to reduce overall intensity of the conductive noise which is proportional to the input current. This will also be beneficial and reduce the energy peak that must go from the input C to the loads and L, thus reducing the voltage drop on the ESR. This last point shows that it is important to have a good quality capacitor on the input with low ESR. This can be achieved also placing in parallel multiple capacitors and use technology variations, such as electrolytic for the bulk energy storage C_B (high ESR) and ceramic capacitor C_1, C_2 (low ESR) to reduce the total ESR.

Last but not least, the SYNC option will also help to get a known switching frequency. This may help any filter in the analog subsystems, even if there is a single DC-DC converter. Synchronizing two DC-DC converters also means that the EMI filter will face low frequency signals due to a non synchronized DC-DC converter which may create harmonics with a frequency made out of the difference of the switching frequency.

Conclusions

In this article we have described the SYNC function and how it is used. In particular the EMC perspective benefits have been also shown, making the SYNC pin a valuable feature to be used within high current applications not just to reduce the input current but also to reduce conducted and radiated noise.

Bibliography

[1] www.LaurTec.it: official site where you can download the "EMC Testing" series.

History

Date	Version	Author	Revision	Description
25. July 2020	1.2	Mauro Laurenti	Mauro Laurenti	Minor reformatting and typos corrections.
28. May. 2020	1.1	Mauro Laurenti	Mauro Laurenti	Added a sentence.
15. May. 2020	1.0	Mauro Laurenti	Mauro Laurenti	Original version.